CH7512A DP/eDP to LVDS Converter

FEATURES

- Supports DisplayPort Specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.4
- Support 2 Main Link Lanes at either 1.62Gb/s, 2.7Gb/s , 3.24Gb/s or 5.4Gb/s link rate
- Supports input color depth 6, 8-bit per pixel in RGB format
- Supports Enhanced Framing Mode
- Support VESA and CEA timing standards up to 1920x1080 resolution in 8-bit input with 60Hz refresh rate(1), or with 144Hz refresh rate(2)
- Support dynamic refresh rate switching
- Panel tuning methods support 6-bit + FRC
- Fast and full Link Training for DisplayPort system
- Crystal Free
- Programmable LCD panel power sequence
- Support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS output interface
- Support both OpenLDI and SPWG bit mapping for LVDS application
- Support panel select by GPIO pins control or writing the chip registers.
- Flexible LVDS output pins swapping
- Blank panel during invalid input
- Test Pattern Generator integrated
- Supports PWM. Backlight luminance level control through AUX channel, PWM input pin and BLUP/BLDN pin
- Support OSD display when BLUP/BLDN pins control Backlight Luminance
- Support Chip Power Down control by GPIO pin
- Hot Plug Detection
- Loads Boot ROM automatically upon power up
- Serial BOOT ROM data updated through I2C bus or AUX Channel
- Support power management mechanism through AUX Channel
- EMI reduction capability for DP input and LVDS output. Spread spectrum control is available for transmitting LVDS signal
- Low power consumption
- Offered in a 68-pin QFN package
- Support Pin to Pin compatible with CH7511B*

APPLICATION

- AIO
- Notebook/Pad
- IPC Motherboard

GENERAL DESCRIPTION

Chrontel's CH7512A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the LVDS **(**Low-voltage Differential Signaling). This innovative DisplayPort receiver with an integrated LVDS transmitter is specially designed to target the All-In-One PC and the notebook market segments. Through the CH7512A's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized video data can be seamlessly converted to LVDS, a popular display technology for high-speed serial links in mid/large-sized LCD displays. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7512A is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7512A and the graphic chip.

The CH7512A is designed to meet the DisplayPort Specification 1.2 and Embedded DisplayPort (eDP) Specification version 1.4. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s, 2.7Gb/s, 3.24Gb/s or 5.4Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8 for LVDS output up to 1920x1080@60Hz(1) or 1920x1080@144Hz(2). To comply with GPU's new power saving scheme such as display frame rate reduction, the CH7512A is equipped with the Dynamic Refresh Rate switching method, which can automatically reduce to the low refresh rate supported by the LVDS panel.

The integrated LVDS transmitter supports the single port and the dual ports LVDS outputs. CH7512A supports panel select by GPIO[5, 3:0] pins control. To reduce EMI emission, the CH7512A's LVDS encoder block has incorporated Spread Spectrum control and its spread percentage can be adjusted through the internal registers.

The Backlight On/Off and the PWM are two luminance control functions designed in the CH7512A LVDS power control module. The brightness control commands sent through AUX Channel can be dynamically translated by CH7512A and converted into LCD backlight control signal. The CH7512A will save the last setting of brightness level into the BOOT ROM and restore it upon power up. The CH7512A can dynamically adjust backlight brightness according to video stream to save power consumption and it supports OSD display in this way.

The CH7512A will immediately convert the DisplayPort signal to LVDS output after DisplayPort Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7512A's configuration settings in the serial BOOT ROM connected to the CH7512A. During system power-up and upon completion of the DisplayPort Link Training through AUX Channel, CH7512A will generate LVDS signal according to the panel power-up timing sequencing stored in the BOOT ROM. Please contact Chrontel for CH7512A's firmware support.

Note:
(1) Supported by CH7512A-BF/ CH7512A-BFI
(2) Supported by CH7512A-BF-H/ CH7512A-BFI-H

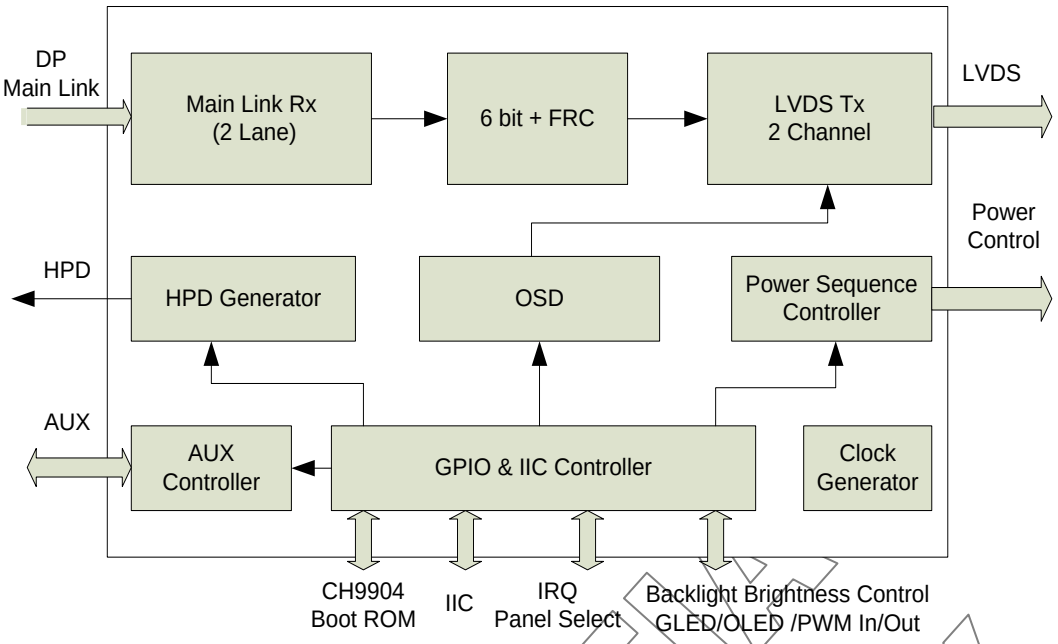

Figure 1: CH7512A Function Block Diagram

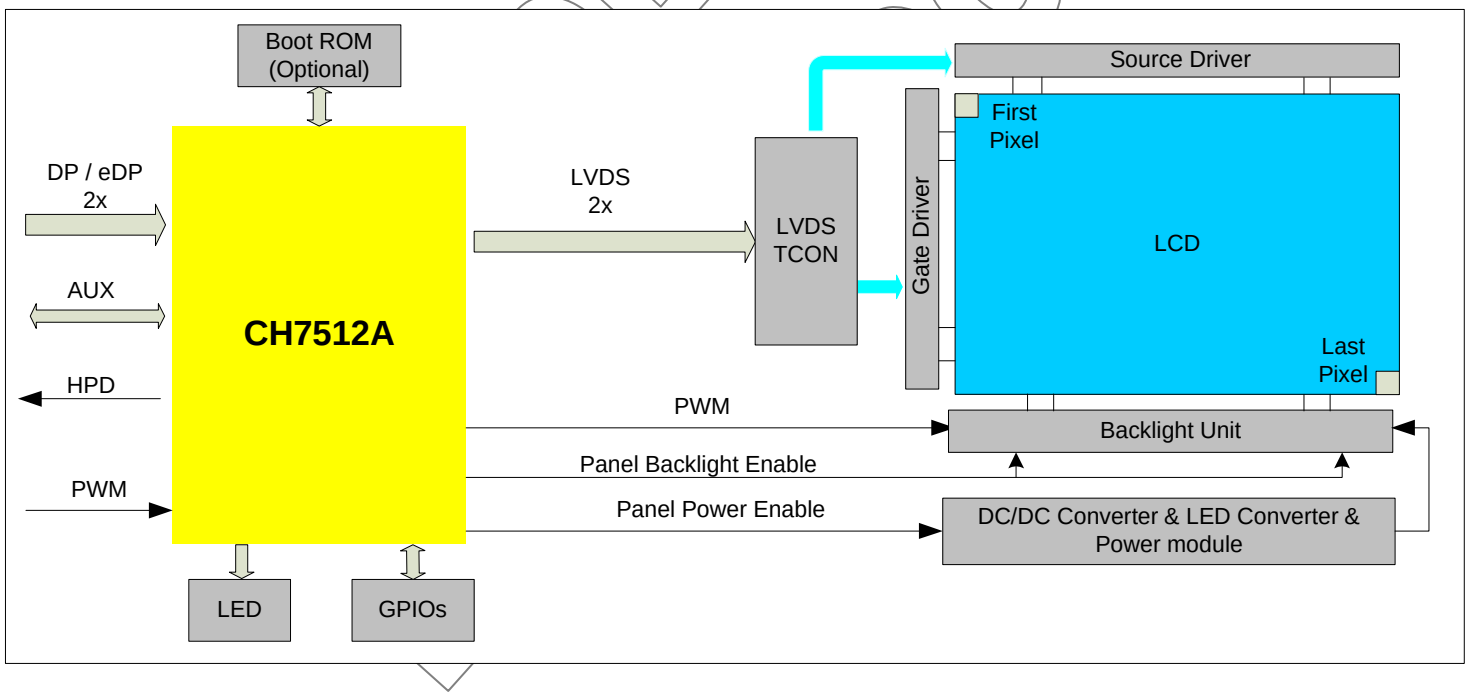

Figure 2: CH7512A Application Diagram

1.0 PIN ASSIGNMENT

1.1 Package Diagram

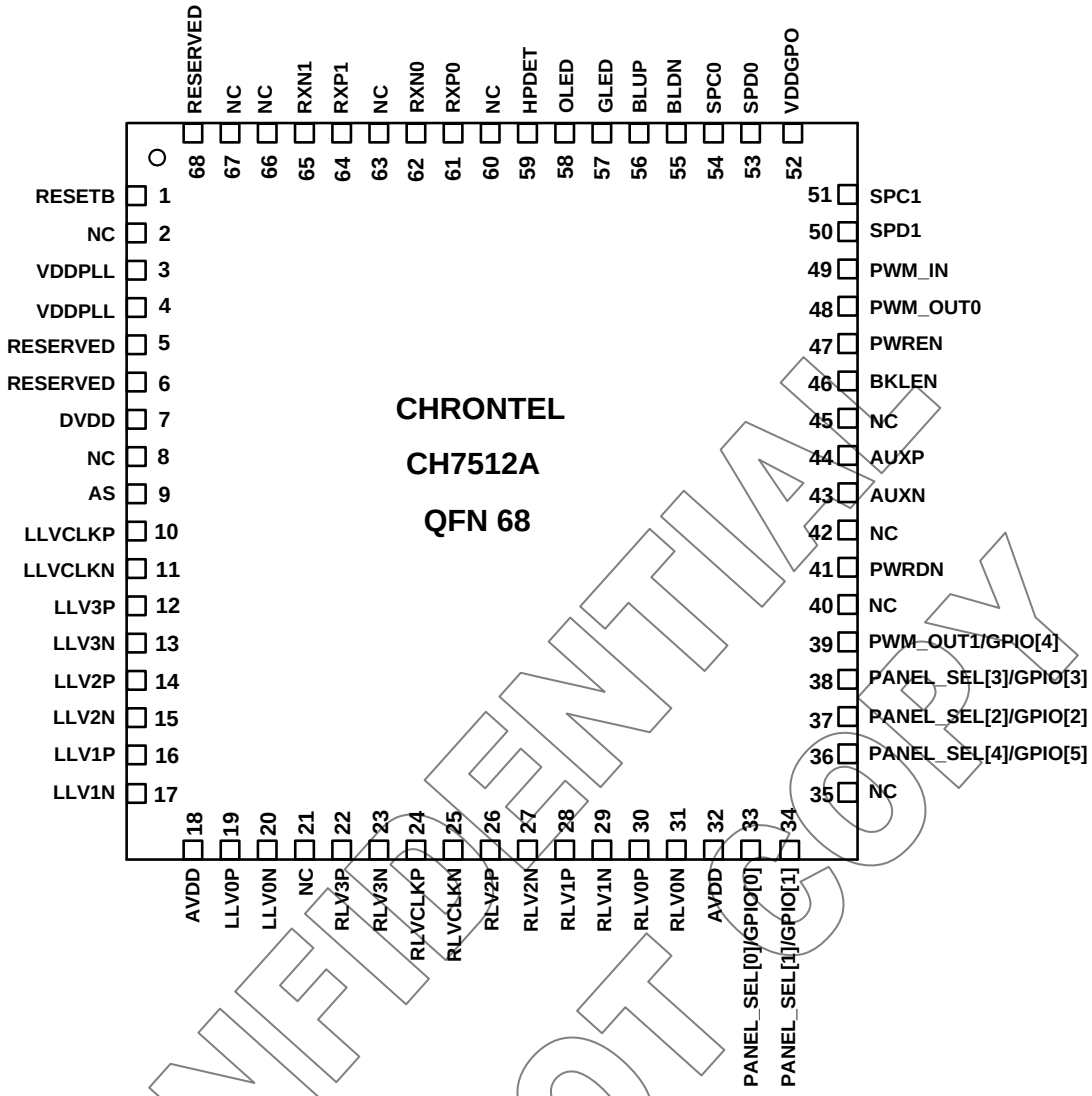

Figure 3: CH7512A 68-pin QFN pin out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	RESETB	**Reset Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high (3.3/1.8/1.2V), reset is controlled through the serial port register. It should be pulled high with a 10 KΩ resistor and a 0.1µF capacitor.
2,8,21,35,40,42,45,60,63,66,67		NC	**Not Connected**
5,6		RESERVED	**Reserved Pins** Capacitors should be connected between these pins and ground.
9	In	AS	**I2C Slave Device Address Selection**
10~17, 19,20, 22~31	Out	LLVCLKP/N, RLVCLKP/N LLV [3:0] P/N RLV [3:0] P/N	**LVDS Output**
33~34, 36~38	In	PANEL_SEL[4:0]/GPIO[5,3:0]	**Panel Select Control Signals** These pins could be pulled high (10 KΩ resistor to +3.3V) or low forming into 32 different combinations. Every combination can match with one panel type.
39	Out	PWM_OUT1	**PWM Output for Backlight Brightness Dimming** PWM Duty Cycle Range: 0~100%(32 steps by default) The output Frequency from PWM_OUT1 can be up to 430KHz. Voltage level is 3.3V. Bypass PWM input, and while in bypass mode, frequency of PWM_OUT1 can be up to 1MHz.
41	In	PWRDN	**Power Down Control** CH7512A enters/exit power down state when receiving active low pulse (0V) from this pin.
43,44	In/Out	AUXP, AUXN	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
46	Out	BKLEN	**LCD Panel Backlight Enable** Enable backlight of LCD panel (3.3V)
47	Out	PWREN	**LCD Panel Power Enable** Enable LCD panel VDD (3.3V)
48	Out	PWM_OUT0	**PWM Output for Backlight Brightness Dimming / Bypass PWM_IN** PWM Duty Cycle Range: 0~100%(32 steps by default) The output Frequency from PWM_OUT0 can be up to 430KHz. Voltage level is 3.3V. Bypass PWM input, and while in bypass mode, frequency of PWM_OUT0 can be up to 1MHz.
49	In	PWM_IN	**Backlight brightness PWM input** The input PWM signal will be bypassed to either of the two PWM_OUT pins The input frequency to PWM_IN can be up to 1MHz. Voltage level is 3.3V.
50	In/Out	SPD1	**Serial Port Data Input/Output for Chip BOOT ROM/EDID** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4KΩ - 9 KΩ pull up resistor to 3.3V.
51	Out	SPC1	**Serial Port Clock Output for Chip BOOT ROM/EDID** This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4KΩ - 9KΩ pull up resistor to 3.3V.
53	In/Out	SPD0	**Serial Port Data Input/Output for Register Map** This pin is used to access CH7512A internal registers. It functions as the bi-

Pin #	Type	Symbol	Description
			directional data pin of the serial port and operates with input from 0 to 3.3V. Output is driven from 0 to 3.3V. This pin requires an external 2KΩ - 8 KΩ pull up resistor to 3.3V.
54	In	SPC0	**Serial Port Clock Input for Register Map** This pin is used to access CH7512A internal registers. It functions as the clock input of the serial port and operates with input from 0 to 3.3V. This pin requires an external 2KΩ - 8 KΩ pull up resistor to 3.3V.
55	In	BLDN	**Decrement Backlight Brightness Input**
56	In	BLUP	**Increment Backlight Brightness Input**
57	Out	GLED	**Green LED Control** This pin indicates CH7512A in normal power and mode status. Its output voltage is 3.3V.
58	Out	OLED	**Orange LED Control** This pin indicates CH7512A in abnormal power and mode status. Its output flickers from 0 or 3.3V.
59	Out	HPDET	**Hot Plug Detect** This output pin is used as the connection detection by a DisplayPort Source system. It generates interrupt pulse as defined by DisplayPort standard. The output voltage is 3.3V. A 100 kΩ resistor should be connected between this pin and GND. It should be linked to DisplayPort source.
68		RESERVED	**Reserved Pin** This pin should be left open in the application.
61,62 64,65	In	RXP/N[1:0]	**Main Link Lane Input** These pins accept two AC-coupled differential pairs signals from the DisplayPort transmitter.
3,4	Power	VDDPLL	**Analog Power Supply (1.2~1.8V)**
7	Power	DVDD	**Digital Power Supply (1.2~1.8V)**
18,32,52	Power	AVDD, VDDGPO	**LVDS Driver Power Supply and GPO Power Supply (3.3V)**
Thermal Exposed Pad	Power	GND	**Power Ground**

2.0 PACKAGE DIMENSIONS

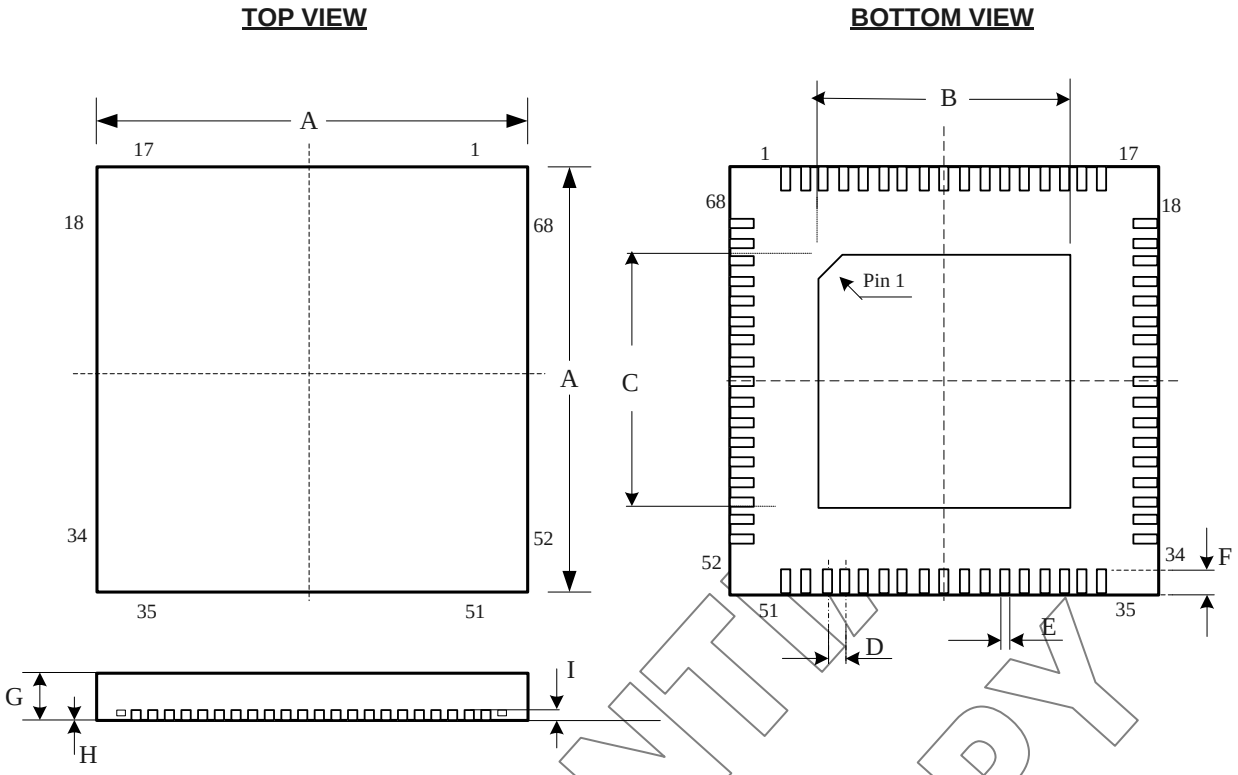

Figure 4: 68 Pin QFN Package (8x8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
68 (8x8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.90	4.30	4.30	0.40 BSC	0.15	0.30	0.70	0	0.203 REF
	MAX	8.10	4.50	4.50		0.25	0.50	0.80	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207

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ORDERING INFORMATION

Part Number	Package Type	MAX Resolution	Operating Temperature Range	Minimum Order Quantity
CH7512A-BF	68QFN, Lead-free,	1920x1080@60Hz	Commercial : 0 to 70°C	260/TRAY
CH7512A-BFI	68QFN, Lead-free	1920x1080@60Hz	Industrial : -40 to 85°C	260/TRAY
CH7512A-BF-H	68QFN, Lead-free	1920x1080@144Hz	Commercial : 0 to 70°C	260/TRAY
CH7512A-BFI-H	68QFN, Lead-free	1920x1080@144Hz	Industrial : -40 to 85°C	260/TRAY

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